Abstract of the Disclosure

A method and apparatus for improving output skew across the data bus of a synchronous integrated circuit device. The device includes a clock input buffer that receives a system clock signal and generates a buffered clock signal, a delay line that receives the buffered clock signal and generates a delayed clock signal, and an output circuit including output signal paths for outputting the output signals synchronously with the system clock signal by using the delayed clock signal. At least one of the output signal paths includes a delay circuit and an output buffer. Each delay circuit provides a programmable delay to the delayed clock signal to generate a unique delayed clock signal used to clock an output signal into the respective output buffer. By programming the delays based upon output skew, the output skew can be improved.